B2 cont

During testing of the Flash EPROM cell, the bypass switch 50 is closed thereby bypassing transistors 46a-46n. This reduces the voltage observed at the cathode of the protective diode 38 by $n*V_t$. Thus, the margin erase voltage is given by:

$$V_{ME} = V_{bd} + V_t.$$

IN THE CLAIMS

Please amend the Claims as follows.

B3

1. (TWICE AMENDED) A method of margin erasing memory cells in a testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses charge pump circuitry to develop both a normal erase voltage used in normal operation and a margin erase voltage used in said testing procedure wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

Please cancel Claim 2.

B4

14. (TWICE AMENDED) A method of margin erasing memory cells in a testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses an internal charge pump circuit to develop both a normal erase voltage used in normal operation and a margin erase voltage used in said testing procedure and wherein said margin erase voltage applied to said memory cells during said margin

B4 cont'd

erasing is reduced over said normal erase voltage by bypassing series connected voltage dropping components wherein said voltage is reduced by n times a voltage of one of said voltage dropping components where n is the number of voltage dropping components connected in said series.

Please cancel Claim 15.

B5

26. (TWICE AMENDED) A flash EPROM memory device comprising:

a charge pump circuit;

a protective diode having a cathode and an anode wherein said cathode of said protective diode is connected to said charge pump circuit;

a plurality of series connected voltage dropping devices wherein a drain of a first of said plurality of series connected voltage dropping devices is connected to said anode of said protective diode;

a bias current source connected to a source of said last of said plurality of series connected voltage dropping devices; and

a bypass switch to bypass one or more of said series connected voltage dropping devices wherein during normal operation of said flash EPROM memory device, said plurality of series connected voltage dropping devices is not bypassed to provide a normal erase voltage and wherein during margin erasing, said plurality of series connected voltage dropping devices is bypassed thereby providing a margin erase voltage that is lower than said normal erase voltage.